

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Packaged in a Narrow 0.3" 24-Pin DIP
- Direct Parallel Load of All 12 Bits for High Data Throughput
- On-Chip Latches for Both DACs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 0.2% Typically
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Robotics/Process Control
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION [†]

		-PACKAGE		
RELATIVE ACCURACY	GAIN ERROR (+5V or +15V)	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8221AW	DAC8221EW	—
±1/2 LSB	±2 LSB	—	—	DAC8221GP
±1 LSB	±4 LSB	—	DAC8221FW	DAC8221HP
±1 LSB	±4 LSB	—	DAC8221FP	DAC8221HST

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

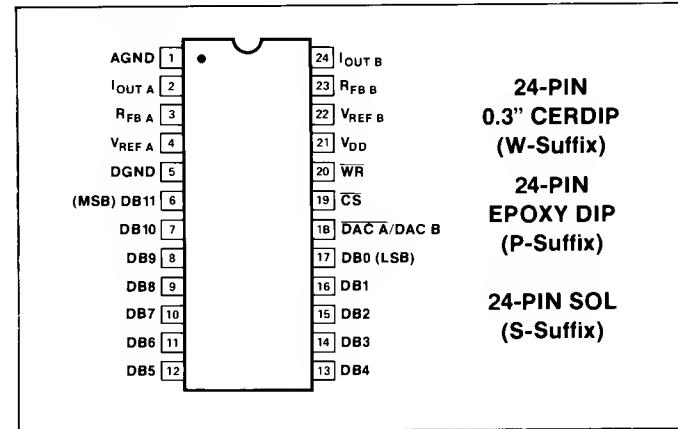
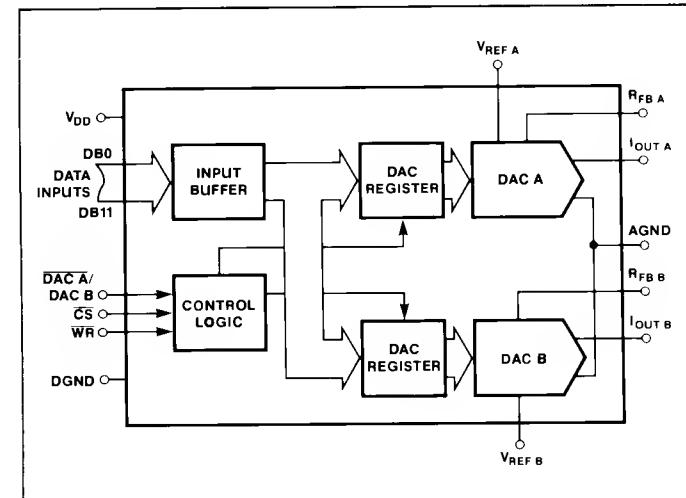
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The DAC-8221 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. This device is electrically similar to DAC-8212 with improved microprocessor interface timing and is packaged in a narrow 0.300" DIP. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8221 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8221 operates on a single supply from +5V to +15V. Maximum power dissipation with 0V and +5V logic levels

and a +5V supply is less than 0.5mW. The DAC-8221 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit or wider bus systems. With WR and CS lines at logic LOW, the input data registers are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by DAC A/DAC B control input. For applications requiring double-buffering, see the DAC-8222.

PIN CONNECTIONS

FUNCTIONAL DIAGRAM


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DAC-8221

ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
Digital Input Voltage to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
$I_{OUT\ A}, I_{OUT\ B}$ to AGND	-0.3V, $V_{DD} + 0.3\text{V}$
$V_{REF\ A}, V_{REF\ B}$ to AGND	$\pm 25\text{V}$
$V_{RFB\ A}, V_{RFB\ B}$ to AGND	$\pm 25\text{V}$
Operating Temperature Range	
AW Version	-55°C to +125°C
EW, FW, FP Versions	-40°C to +85°C
GP, HP, HS Versions	-0°C to +70°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

PACKAGE TYPE	θ_{JA} (NOTE 1)	θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE:

1. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do not apply voltages higher than V_{OO} or less than GND potential on any terminal except V_{REF} and R_{FB} .
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$ or $+15\text{V}$, $V_{REF\ A} = V_{REF\ B} = +10\text{V}$, $V_{OUT\ A} = V_{OUT\ B} = 0\text{V}$; AGND = DGND = 0V; T_A = Full Temp. Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

DAC-8221					
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX
STATIC ACCURACY					
Resolution	N		12	-	-
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8221A/E/G DAC-8221B/F/H	- -	± 0.2 ± 0.4
Differential Nonlinearity	DNL	All Grades are Monotonic	-	± 0.2	± 1
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8221A/E DAC-8221G DAC-8221B/F/H	- - -	± 0.1 ± 0.4 ± 0.6	± 1 ± 2 ± 4
Gain Temperature Coefficient $\Delta\text{Gain}/\Delta\text{Temperature}$	TCG_{FS}	(Notes 2, 7)	-	± 2	± 5
Output Leakage Current $I_{OUT\ A}$ (Pin 2), $I_{OUT\ B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	$T_A = +25^\circ\text{C}$ T_A = Full Temp. Range	- -	± 1 ± 2
Input Resistance ($R_{REF\ A}, R_{REF\ B}$)	R_{REF}	(Note 9)	8	22	15
Input Resistance Match ($R_{REF\ A}, R_{REF\ B}$)	$\frac{\Delta R_{REF}}{R_{REF}}$		-	± 0.2	± 1
DIGITAL INPUTS					
Digital Input High	V_{INH}	$V_{DD} = +5\text{V}$ $V_{OO} = +15\text{V}$	2.4 13.5	- -	-
Digital Input Low	V_{INL}	$V_{OO} = +5\text{V}$ $V_{OO} = +15\text{V}$	-	-	0.8
-	-	-	-	-	1.5
Input Current	I_{IN}	$V_{IN} = 0\text{V}$ or V_{OO} and V_{INL} or V_{INH}	$T_A = +25^\circ\text{C}$ T_A = Full Temp. Range	± 0.006 ± 0.1	± 1 ± 10
Input Capacitance (Note 2)	C_{IN}	DB0 - DB11 $\bar{WR}, CS, \bar{DAC\ A/DAC\ B}$	-	-	10
-	-	-	-	-	15

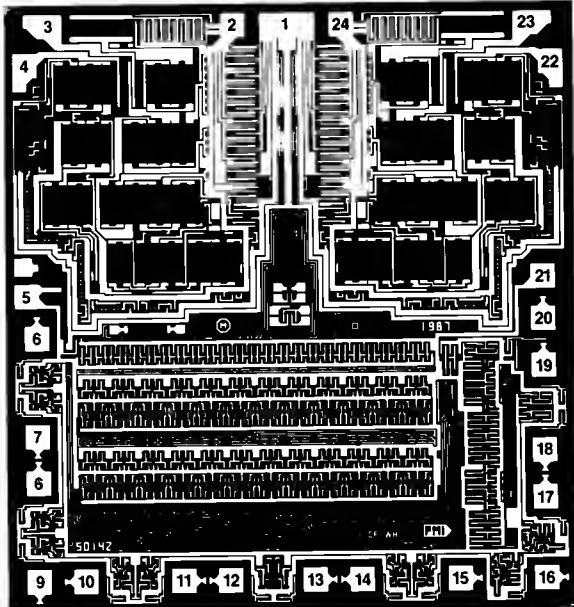
ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF\ A} = V_{REF\ B} = +10V$, $V_{OUT\ A} = V_{OUT\ B} = 0V$; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8221			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
Supply Current	I_{OO}	All Digital Inputs V_{INL} or V_{INH}	—	1	2	mA
		All Digital Inputs 0V or V_{DD}	—	2	100	μA
DC Power Supply Rejection Ratio (Δ Gain/ ΔV_{OO})	PSRR	$\Delta V_{OO} = \pm 5\%$	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{pd}	$T_A = +25^\circ C$	—	—	350	ns
Current Settling Time (Notes 5, 6)	t_s	$T_A = +25^\circ C$	—	0.45	1	μs
Output Capacitance	$C_{OUT\ A}$	DAC Latches Loaded with 0000 0000 0000	—	30	90	pF
	$C_{OUT\ B}$		—	60	120	
	$C_{OUT\ A}$	DAC Latches Loaded with 1111 1111 1111	—	60	120	
	$C_{OUT\ B}$		—	30	90	
AC Feedthrough at $I_{OUT\ A}$ or $I_{OUT\ B}$	FT_A	$V_{REF\ A}$ to $I_{OUT\ A}$; $V_{REF\ A} = 20V_{p-p}$; $f = 100kHz$; $T_A = +25^\circ C$	—	—	-70	dB
	FT_B	$V_{REF\ B}$ to $I_{OUT\ B}$; $V_{REF\ B} = 20V_{p-p}$; $f = 100kHz$; $T_A = +25^\circ C$	—	—	-70	
SWITCHING CHARACTERISTICS (Notes 2, 3)			$V_{DD} = +5V$		$V_{DD} = +15V$	
			+25°C	-40°C TO +85°C (Note 8)	-55°C TO +125°C	ALL TEMPS (Note 10)
Chip Select to Write Set-Up Time	t_{CS}		130	160	160	70 ns MIN
Chip Select to Write Hold Time	t_{CH}		0	0	0	0 ns MIN
DAC Select to Write Set-Up Time	t_{AS}		120	140	160	70 ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0 ns MIN
Data Valid to Write Set-Up Time	t_{OS}		190	210	220	90 ns MIN
Data Valid to Write Hold Time	t_{OH}		0	0	0	10 ns MIN
Write Pulse Width	t_{WR}		140	180	170	90 ns MIN

NOTES:

- Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$. Both DAC digital inputs = 1111 1111 1111.
- Guaranteed and not tested.
- See timing diagram.
- From 50% of digital input to 90% of final analog output current. $V_{REF\ A} = V_{REF\ B} = +10V$; OUT A, OUT B load = 100Ω , $C_{EXT} = 13pF$.
- $WR, CS = 0V$; $DB0 - DB11 = 0V$ to V_{OO} or V_{OO} to 0V.
- Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .
- These limits apply for the commercial and industrial grade products.
- Absolute temperature coefficient is approximately $+50ppm/\text{ }^\circ C$.
- These limits also apply as typical values for $V_{OO} = +12V$ with +5V CMOS logic levels and $T_A = +25^\circ C$.

DICE CHARACTERISTICS



DIE SIZE 0.124 x 0.132 inch, 16,368 sq. mils
(3.15 x 3.35 mm, 10.55 sq. mm)

1. AGND	13. DB4
2. I _{OUT} A	14. DB3
3. R _{FB} A	15. DB2
4. V _{REF} A	16. DB1
5. DGND	17. DB0 (LSB)
6. DB11 (MSB)	18. DAC A/DAC B
7. DB10	19. CS
8. DB9	20. WR
9. DB8	21. V _{DD}
10. DB7	22. V _{REF} B
11. DB6	23. R _{FB} B
12. DB5	24. I _{OUT} B

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF} A = V_{REF} B = +10V, V_{OUT} A = V_{OUT} B = 0V; AGND = DGND = 0V; T_A = 25°C.

DAC-8221GBC

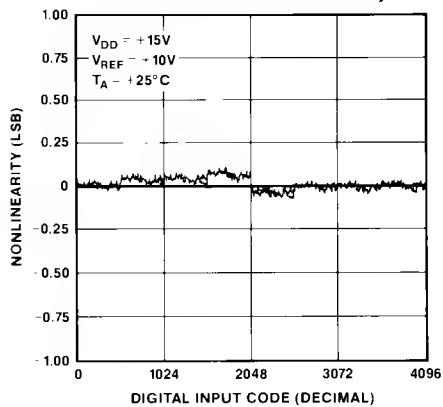
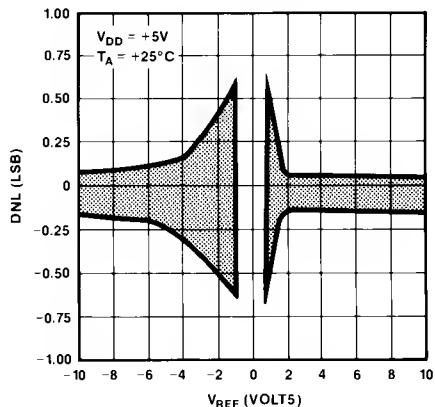
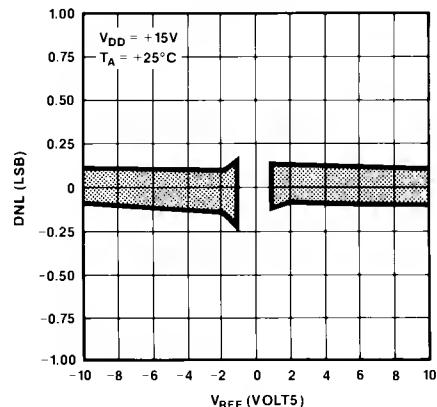
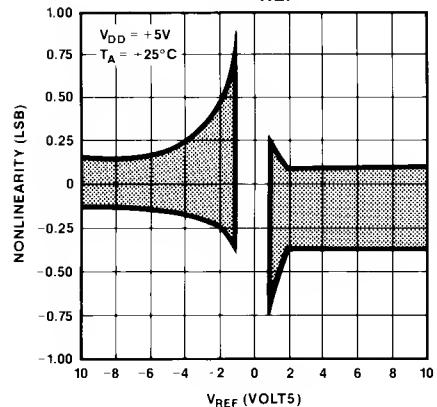
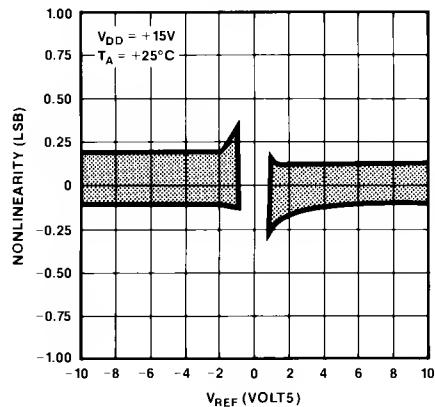
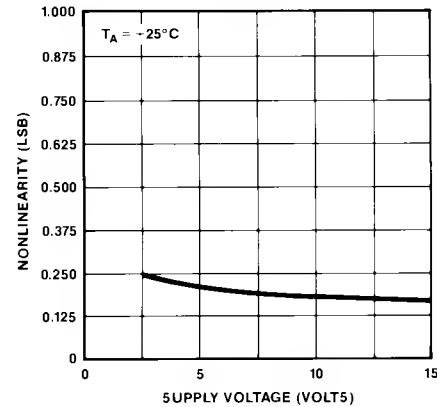
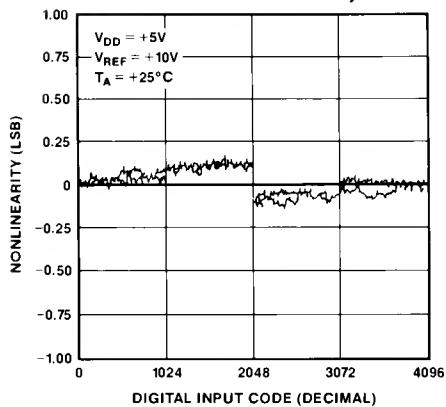
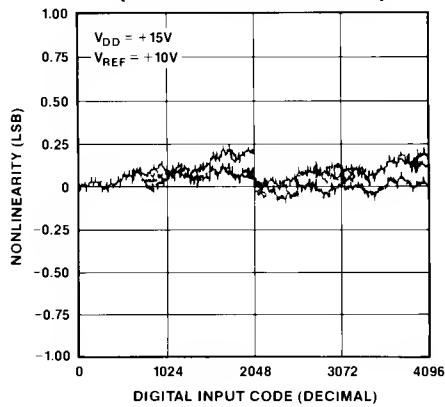
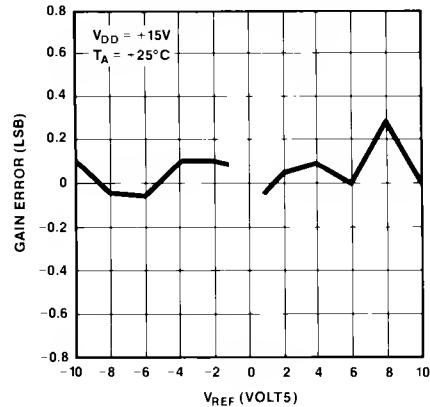
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB MAX
Full Scale Gain Error (Note 1)	G _{FS} E	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage (I _{OUT} A, I _{OUT} B)	I _{LKG}	Digital Inputs = 0000 0000 0000 Pads 2 and 24	±10	nA MAX
Input Resistance (R _{REF} A, R _{REF} B)	R _{REF}	Pads 4 and 22	8/15	kΩ MIN/ kΩ MAX
R _{REF} A, R _{REF} B Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% MAX
Digital Input High	V _{INH}	V _{DD} = +5V V _{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V _{INL}	V _{DD} = +5V V _{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I _{IN}	V _{IN} = 0V or V _{DD} , V _{INL} or V _{INH}	±1	µA MAX
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH} All Digital Inputs 0V or V _{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV _{DD})	PSRR	ΔV _{DD} = ±5%	0.002	%/% MAX

NOTES:

1. Measured using internal R_{FB} A and R_{FB} B.

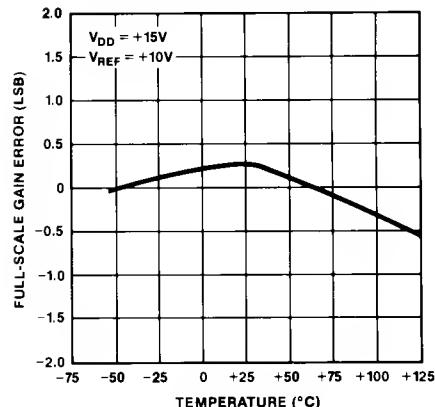
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

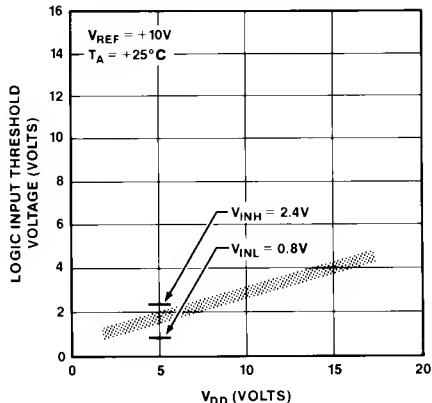
CHANNEL-TO-CHANNEL
MATCHING (DAC A & B
ARE SUPERIMPOSED)DIFFERENTIAL
NONLINEARITY
vs V_{REF} DIFFERENTIAL
NONLINEARITY
vs V_{REF} NONLINEARITY
vs V_{REF} NONLINEARITY
vs V_{REF} NONLINEARITY
vs V_{DD} NONLINEARITY vs CODE
(DAC A & B ARE
SUPERIMPOSED)NONLINEARITY vs CODE AT
 $T_A = -55^{\circ}C, +25^{\circ}C,$
 $+125^{\circ}C$ FOR DAC A & B
(ALL SUPERIMPOSED)ABSOLUTE GAIN ERROR
CHANGE vs V_{REF} 

TYPICAL PERFORMANCE CHARACTERISTICS

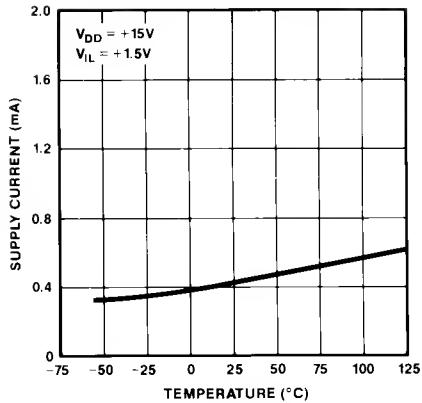
**FULL-SCALE GAIN ERROR
vs TEMPERATURE**



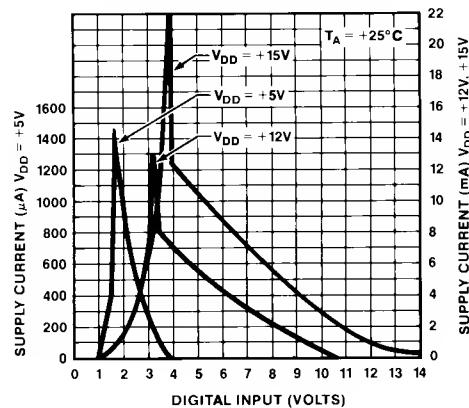
**LOGIC INPUT THRESHOLD
VOLTAGE vs SUPPLY
VOLTAGE (V_{DD})**



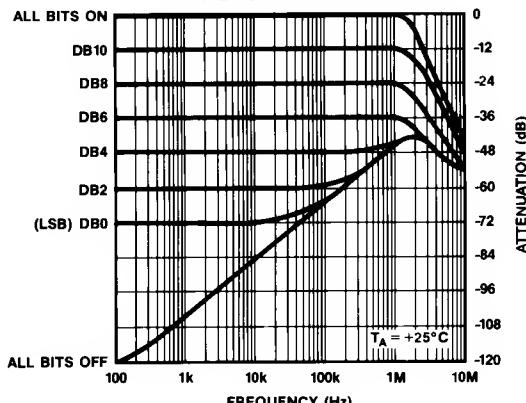
**SUPPLY CURRENT
vs TEMPERATURE**



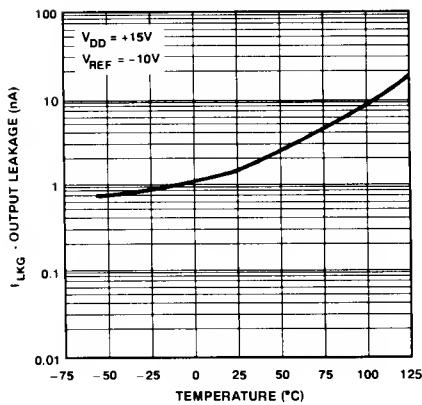
**SUPPLY CURRENT vs
LOGIC INPUT VOLTAGE**



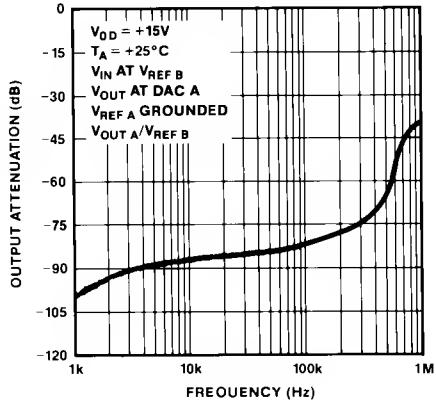
**MULTIPLYING MODE
FREQUENCY RESPONSE
vs DIGITAL CODE**



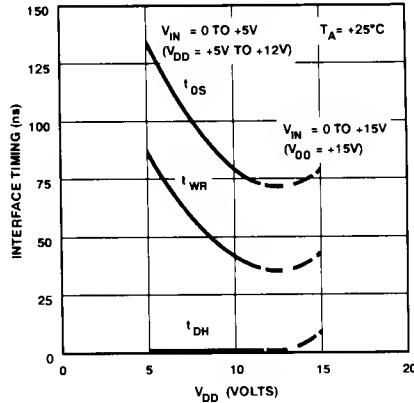
**OUTPUT LEAKAGE CURRENT
vs TEMPERATURE**



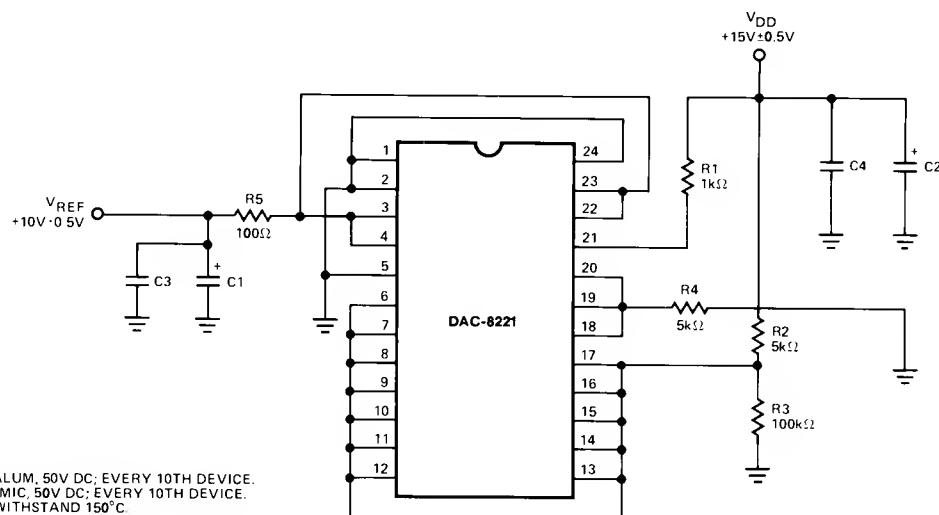
**ANALOG CROSSTALK
vs FREQUENCY**



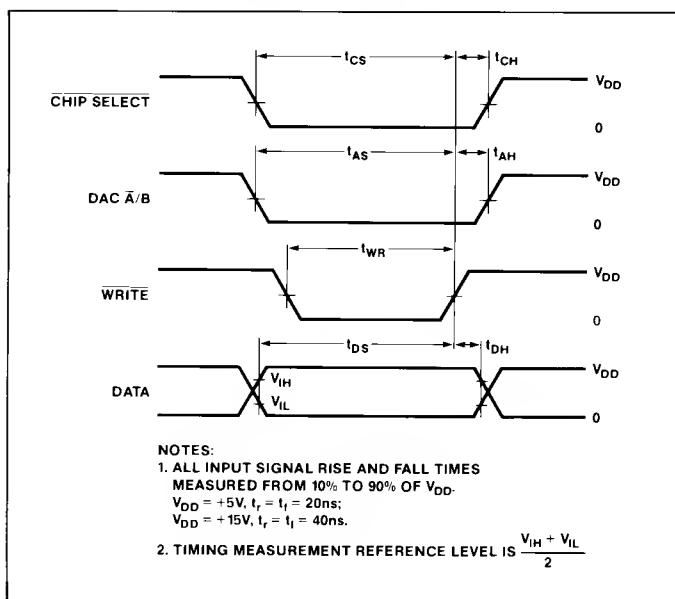
**INTERFACE TIMING
vs V_{DD}**



BURN-IN CIRCUIT



WRITE CYCLE TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight

line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ± 1 LSB may be nonmonotonic. $\pm 1/2$ LSB INL guarantees monotonicity and ± 1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

Refer to PMI 1990/91 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC-8221 incorporates two multiplying 12-bit current output CMOS digital-to-analog converters on one monolithic chip. It contains two highly-stable thin-film R-2R resistor-ladder networks, two 12-bit DAC registers, and one 12-bit input buffer. It also contains the DAC control logic circuitry and 24 single-pole, double-throw NMOS transistor current switches.

Figure 1 shows a simplified circuit for the R-2R ladder and transistor switches for a single DAC. R is typically $11\text{k}\Omega$. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. This presents a constant current load to V_{REF} so that it can be driven by a reference voltage or current, AC or DC (positive or negative). It is recommended that a low temperature-coefficient external R_{FB} resistor be used if a current source is employed. Figure 2 shows a single NMOS transistor switch.

FIGURE 1: Simplified D/A Circuit

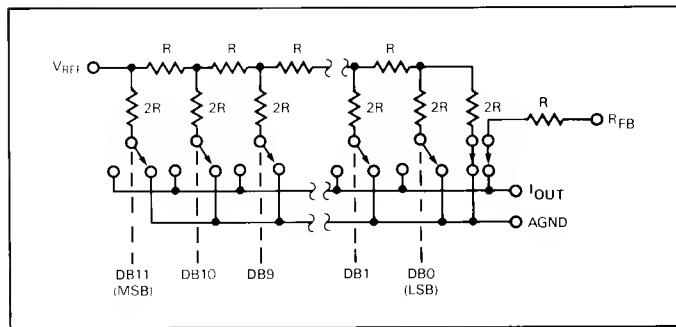
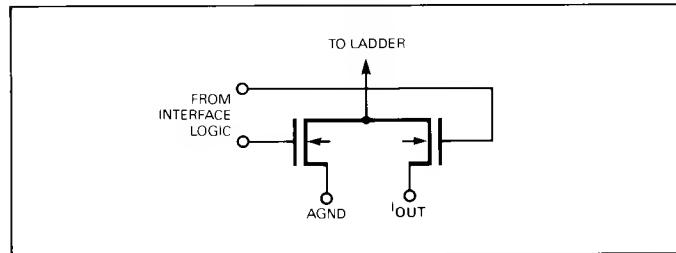


FIGURE 2: N-Channel Current Steering Switch



The binary-weighted currents are switched between I_{OUT} and AGND by the transistor switches. Selection between I_{OUT} and AGND is determined by the digital input code. It is important to keep the voltage difference between I_{OUT} and AGND terminals as close to zero as practical to preserve data sheet limits. It is easily accomplished by connecting the DAC's AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The amplifier's feedback resistor can be eliminated by connecting the op amp's output directly to the DAC's R_{FB} terminal (by using the DAC's internal feedback resistor, R_{FB}), see Figure 6. The amplifier also provides the current-to-voltage conversion for the DAC's output current.

The output voltage is dependent on V_{REF} and the digital input code and is given by:

$$V_{\text{OUT}} = -V_{\text{REF}} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90pF (all digital inputs low) to 120pF (all digital inputs high).

To ensure accuracy over the full operating temperature range, a permanently turned "ON" MOS transistor switch was included in series with the feedback resistor (R_{FB}) and the R-2R ladder's terminating resistor (see Figure 1). The gates of these NMOS transistors are internally connected to V_{DD} and will be turned "OFF" (open) when V_{DD} is not applied. If an op amp uses the DAC's R_{FB} resistor to close its feedback loop, then V_{DD} must be applied before or at the same time as the opamp's supply; this will ensure that the op amp's feedback loop will not be "open-circuited" and swing to either rail. In addition, some applications require the DAC's ladder resistance to fall within a certain range and are measured at incoming inspection; V_{DD} must be applied before these measurements can be made.

DIGITAL SECTION

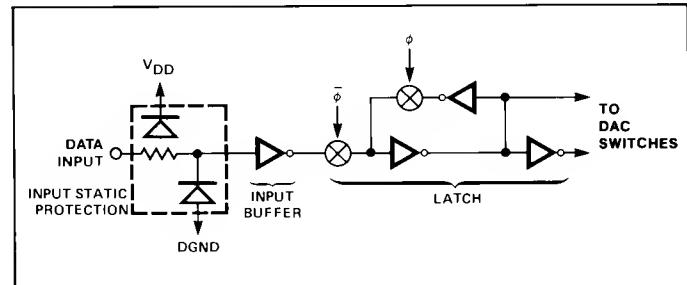
The DAC-8221's digital inputs are TTL compatible at $V_{\text{DD}} = +5\text{V}$ and CMOS compatible at $V_{\text{DD}} = +15\text{V}$. They were designed to convert TTL and CMOS input logic levels into voltage levels that will drive the internal circuitry. The DAC-8221 can use $+5\text{V}$ CMOS logic levels with $V_{\text{DD}} = +12\text{V}$; however, supply current will rise to approximately $5\text{-}6\text{mA}$.

Figure 3 shows the digital input structure for one bit. This circuit drives the DAC register. Digital controls ϕ and $\bar{\phi}$ shown are generated from the DAC's input control logic circuitry.

The digital inputs are electrostatic-discharge (ESD) protected with two internal distributed diodes as shown in Figure 3; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA .

The digital inputs are CMOS inverters and draw supply current when operating in their linear region. Using a $+5\text{V}$ supply, the linear region is between $+1.2\text{V}$ to $+2.8\text{V}$ with current peaking at $+1.8\text{V}$. Using a $+15\text{V}$ supply, the linear region is between $+1.8\text{V}$ to $+12\text{V}$ (current peaking at $+3.9\text{V}$). It is recommended that the digital inputs be operated as close to the power supply voltage and DGND as is practically possible; this will keep supply currents to a minimum. The DAC-8221 may be operated with any supply voltage between the range of $+5\text{V}$ to $+15\text{V}$ and still perform to data sheet limits.

FIGURE 3: Digital Input Structure For One Bit



INTERFACE CONTROL LOGIC INFORMATION

DAC SELECTION

Both DAC registers share a common 12-bit input port. The control input (DAC A/DAC B) selects which DAC can accept data from the input port.

MODE SELECTION

Inputs \overline{CS} and \overline{WR} control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When \overline{CS} and \overline{WR} are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to activity on DB0—DB11 pins.

HOLD MODE

The selected DAC register retains the data which was present on DB0—DB11 pins just prior to \overline{CS} or \overline{WR} assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

DAC A/ DAC B	\overline{CS}	\overline{WR}	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

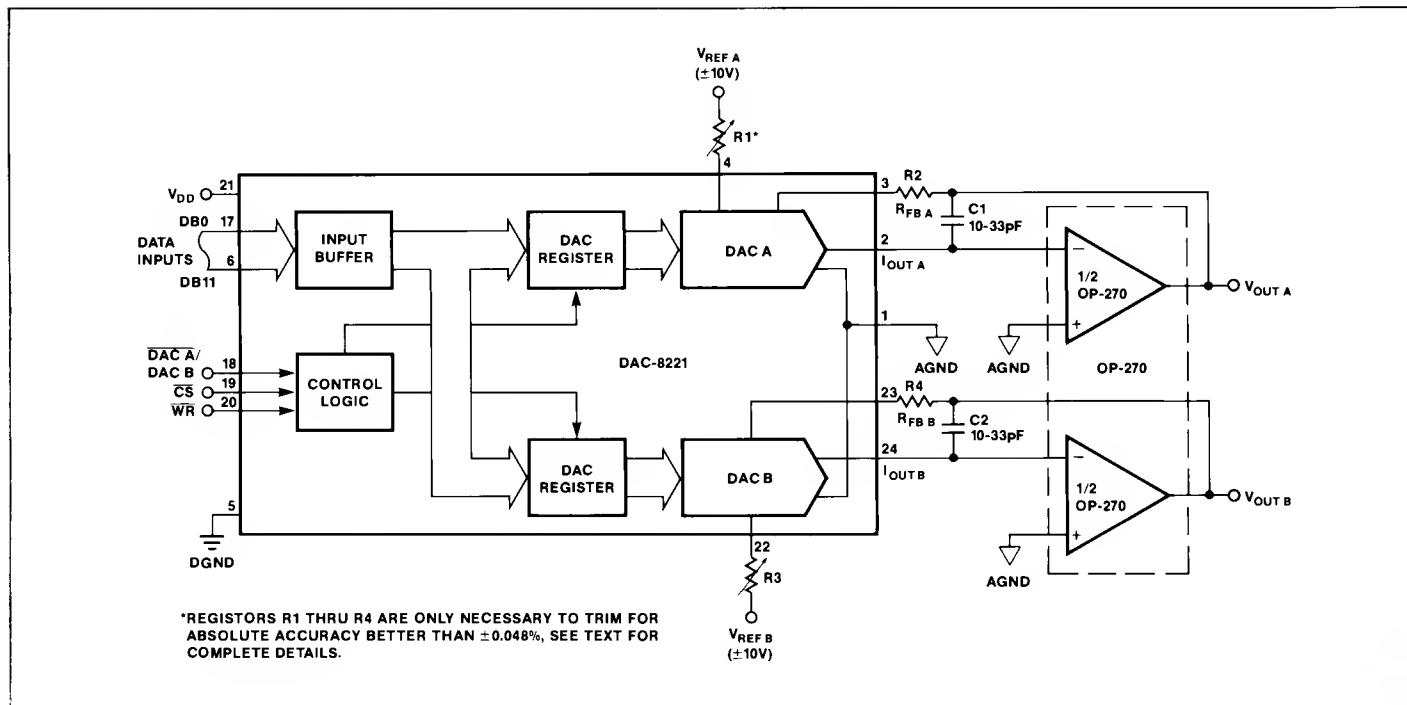
Figure 4 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8221 and OP-270 dual op amp (use two OP-42s for applications requiring higher speeds). Table 1 shows the corresponding code table. Table 3 shows the recommended values for R1, R2, R3, and R4. Low temperature-coefficient (approximately 50ppm/ $^{\circ}$ C) resistors or trimmers should be used. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device where $V_{REF} = \pm 10V$ is 0.048%, and 0.097% for the low grade. Capacitors C1 and C2 provide phase compensation to reduce overshoot and ringing when high-speed op amps are used.

TABLE 1: Unipolar Binary Code Table (Refer to Figure 4)

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB
1111 1111 1111	$-V_{REF} \left(\frac{4095}{4096} \right)$
1000 0000 0000	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{1}{2} V_{REF}$
0000 0000 0001	$-V_{REF} \left(\frac{1}{4096} \right)$
0000 0000 0000	0V

NOTE:
 $1 \text{ LSB} = (2^{-12}) (V_{REF}) = \frac{1}{4096} (V_{REF})$

FIGURE 4: Dual DAC Unipolar Operation (2-Quadrant Multiplication)



DAC-8221

FIGURE 5: Dual DAC Bipolar Operation (4-Quadrant Operation)

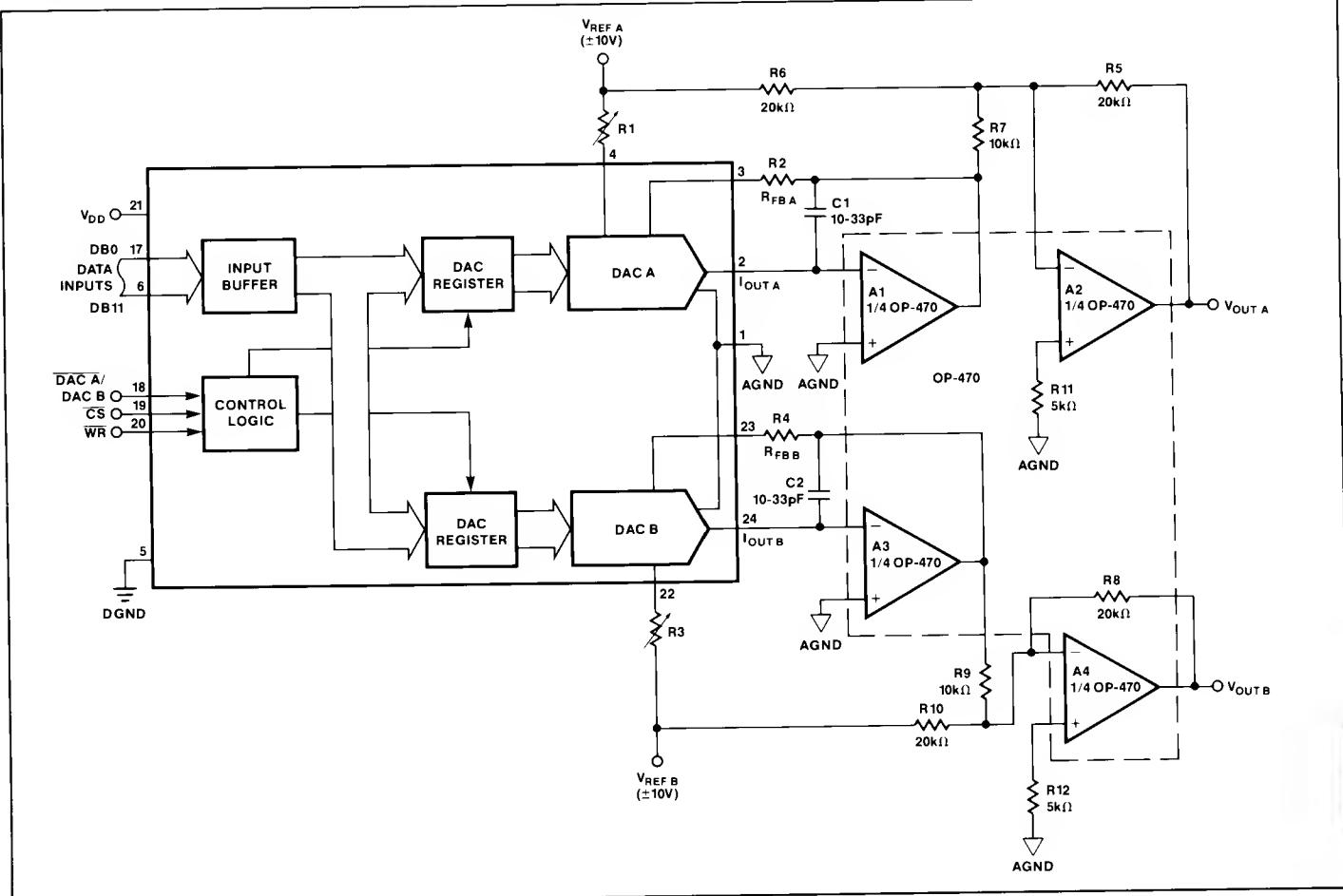


TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 5)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB	
1111 1111 1111		$+V_{REF} \left(\frac{2047}{2048} \right)$
1000 0000 0001		$+V_{REF} \left(\frac{1}{2048} \right)$
1000 0000 0000		0V
0111 1111 1111		$-V_{REF} \left(\frac{1}{2048} \right)$
0000 0000 0000		$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTE:

$$1 \text{ LSB} = (2^{-11}) (V_{REF}) = \frac{1}{2048} (V_{REF})$$

TABLE 3: Recommended Trim Resistor Values vs Grade for Figures 4 and 5

TRIM RESISTOR	FW/HP	AW/EW/GP
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

Full-scale adjustment is achieved by loading the appropriate DAC's digital input with 1111 1111 1111 code and adjusting R1 (or R3 for DAC B) so that:

$$V_{OUT} = V_{REF} \times (4095/4096)$$

If R1, R2, R3, and R4 are not used, then full-scale is adjusted by varying V_{REF} voltage. Zero adjustment is performed by loading the DAC's digital input with 0000 0000 0000 code and adjusting the op amp's offset voltage to 0V. It is recommended that the op amp offset voltage be less than 10% of 1 LSB ($244\mu V$), over the operating temperature range of interest. This will ensure the DAC's monotonicity and minimize gain and linearity errors.

BIPOLAR OPERATION

The bipolar (offset binary) 4-quadrant configuration using the DAC-8221 is shown in Figure 5, and the corresponding code is shown in Table 2. The circuit makes use of the OP-470, a quad op amp (use four OP-42s for applications requiring higher speeds).

Again, resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = \pm 10V$ is 0.048%, and 0.097% for the low grade. See Table 3 for the recommended values. If they are used, then low temperature-coefficient (approximately 50ppm/ $^{\circ}C$) resistors or trimmers should be used.

If resistors R1 thru R4 are omitted, then R5, R6, R7 (R8, R9, and R10 for DAC B) should be ratio-matched to 0.01% to keep gain error within data sheet limits. They should also have matching temperature-coefficient characteristics if operating over the full temperature range.

Zero-output is adjusted by loading the appropriate DAC's digital input with 1000 0000 0000 code and varying R1 (R3 for

DAC B) so that $V_{OUT A}$ (or $V_{OUT B}$) equals 0V. If R1, R2 (R3, R4 for DAC B) are omitted, then zero output is adjusted by varying R6, R7 ratios (R9, R10 for DAC B). Full-scale is set by loading the appropriate DAC's digital inputs with 1111 1111 1111 code and varying R5 (R8 for DAC B) or V_{REF} .

SINGLE SUPPLY OPERATION**CURRENT SWITCHING MODE**

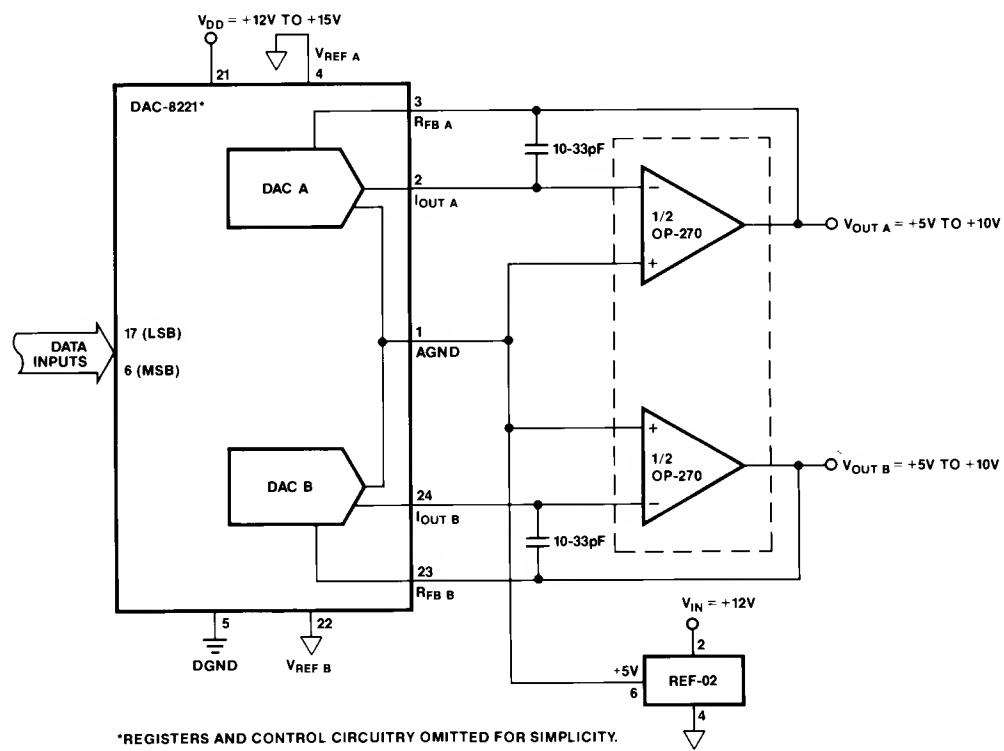
Because the DAC-8221's R-2R resistor-ladder terminating resistor is internally connected to AGND, it lends itself well for single supply operation in the current steering mode configuration. This means that AGND can be raised above system ground as shown in Figure 6. The output voltage will swing between +5V and +10V depending on the digital input code.

The output expression is given by:

$$V_{OUT} = V_{OS} + (D/4096) (V_{OS})$$

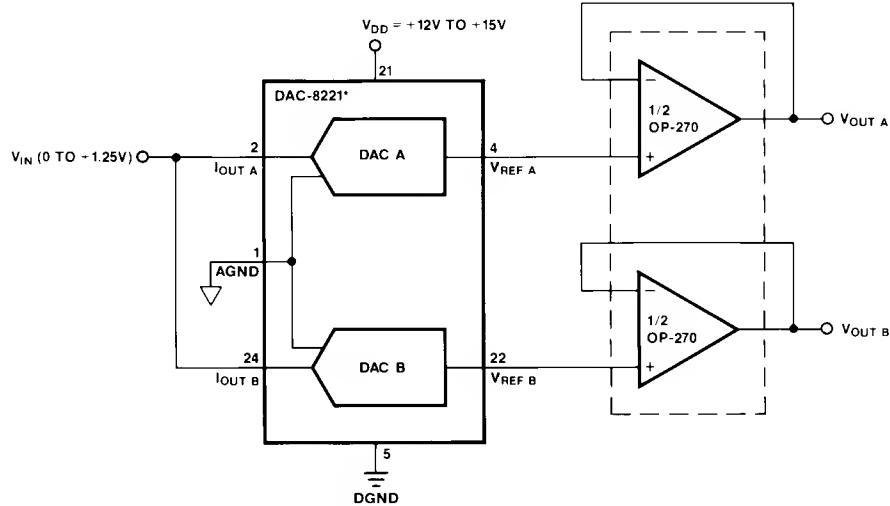
where V_{OS} = Offset Reference Voltage (+5V in Figure 6)
 D = Decimal Equivalent of the Digital Input Word

FIGURE 6: Single Supply Operation (Current Switching Mode)



DAC-8221

FIGURE 7: Single Supply Operation (Voltage Switching Mode)



VOLTAGE SWITCHING MODE

Figure 7 shows the DAC-8221 in another single supply configuration. The R-2R ladder is used in the voltage switching mode and functions as a voltage divider. The output voltage (at the V_{REF} pin) exhibits a constant impedance R (typically $11k\Omega$) and must be buffered by an op amp. The R_{FB} pins are not used and are left open. The reference input voltage must be maintained within $+1.25V$ of AGND, and V_{DD} between $+12V$ and $+15V$; this ensures that device accuracy is preserved.

The output voltage expression is given by:

$$V_{OUT} = V_{REF} (D/4096)$$

where D = Decimal Equivalent of the Digital Input Word

The PC board ground plane can be used for the single point ground if the device socket connection is not practical. If neither of these connections are practical or allowed, then the DAC-8221 should be placed as close as possible to the system's single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC-8221 should be well filtered and regulated. Local supply decoupling consisting of a 1 to $10\mu F$ tantalum capacitor in parallel with a $0.1\mu F$ ceramic is highly recommended. The capacitors should be connected between V_{DD} and DGND and at the device socket.

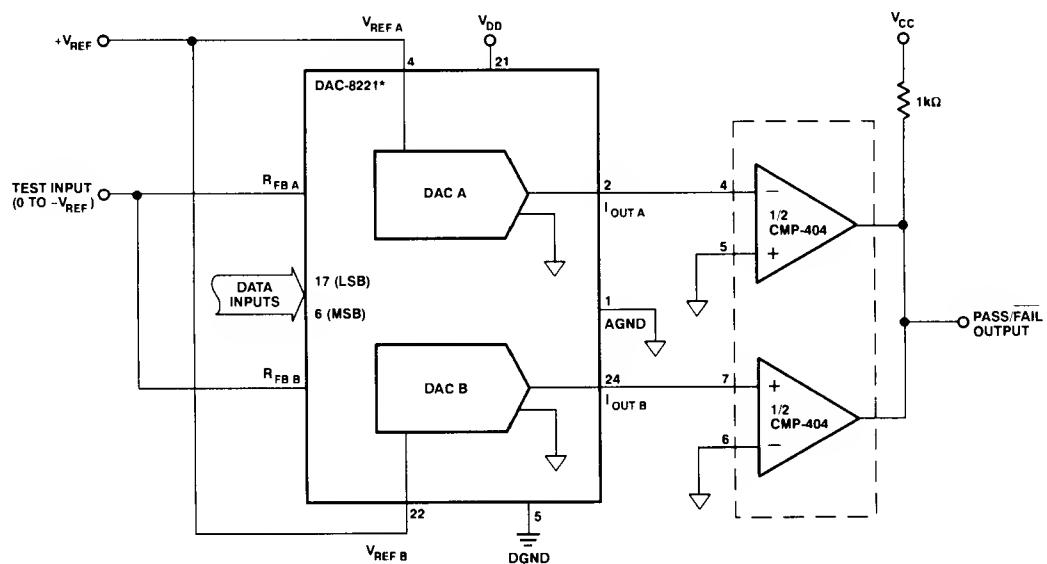
APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have low impedance.

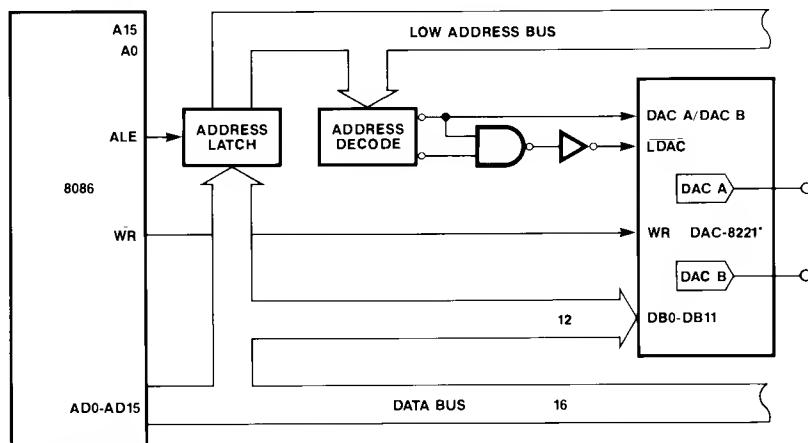
To reduce digital transients from appearing at the analog output, the DAC-8221's AGND and DGND pins should be tied together at the device socket. This common point then becomes the single ground point connection. AGND and DGND is then brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

FIGURE 8: Digitally-Programmable Window Detector (Upper/Lower Limit Detector)



*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

FIGURE 9: DAC-8221 To 8086 Interface



*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

DAC-8221

FIGURE 10: DAC-8221 To 68000 Interface

